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CS548 Double Pulse Testing

Summary

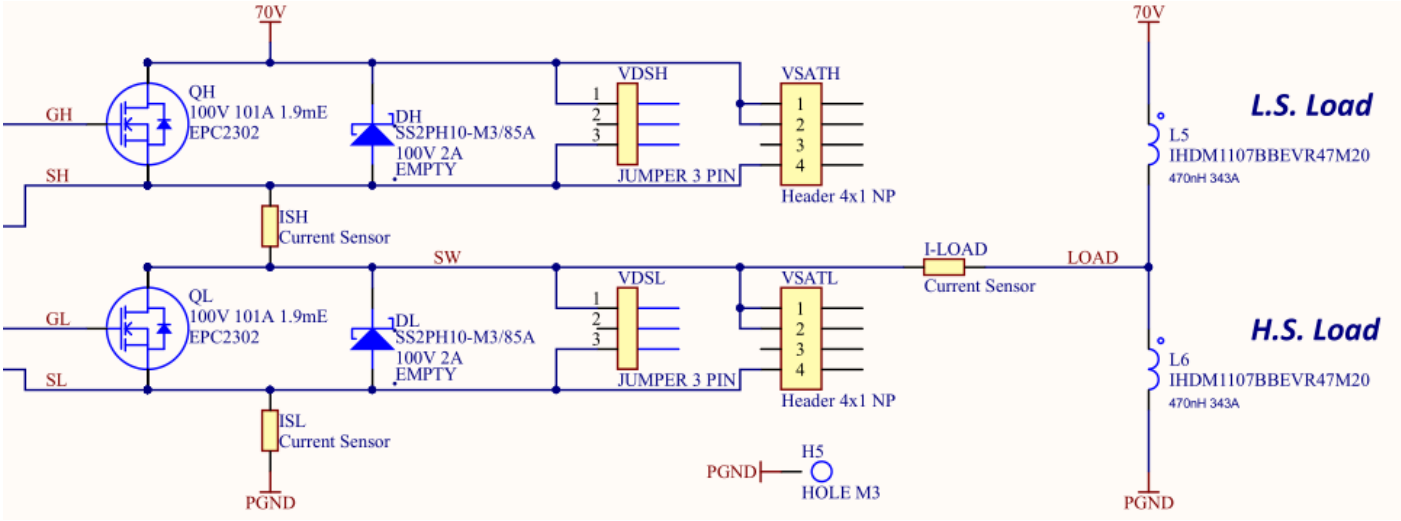
The CS548 isolated-channel oscilloscope can be used for Double Pulse Testing (DPT). This white paper illustrates the measurements that can be made, and how to interpret them. This paper should be read in conjunction with the *CS1501 Insertion Inductance* white paper, which identified the insertion inductance of the CS1501 1 mΩ current sensor to be 163 pH.

Equipment Used

We used the following equipment:

CS1097 GaN half bridge DPT tester

The CS1097 is a GaN half bridge with footprints for the CS1501 current sensor in the 'Source' of both upper and lower transistors. Sensor locations are ISH & ISL in circuit:



The CS1097 is set up with EPC2304 GaN FETs (240V transient, 260A pulsed, 3.1mOhmtyp) and bus voltage set to 40Vdc. The Double Pulse Test is run on High Side transistor QH with 470nH (DCR 0.22mΩ, 343A sat) load inductor fitted from the switch node to PGND, L6.

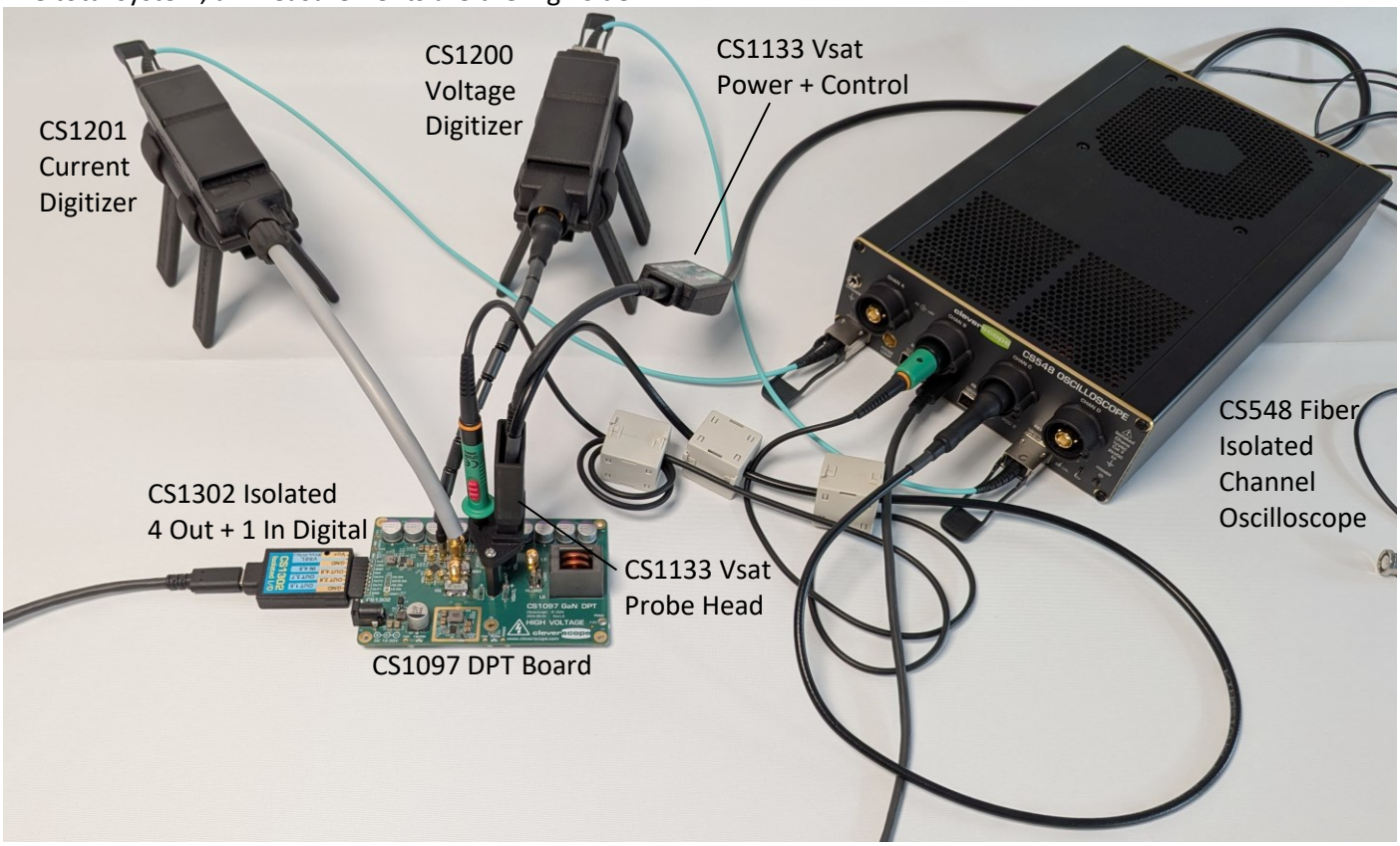
We used the Pulse Accumulate mode, and repeating the DPT 10+ times. Resolutions of sub ns are achieved. The period between DPT shots is arbitrary, we used 100msec to keep device dissipation low.

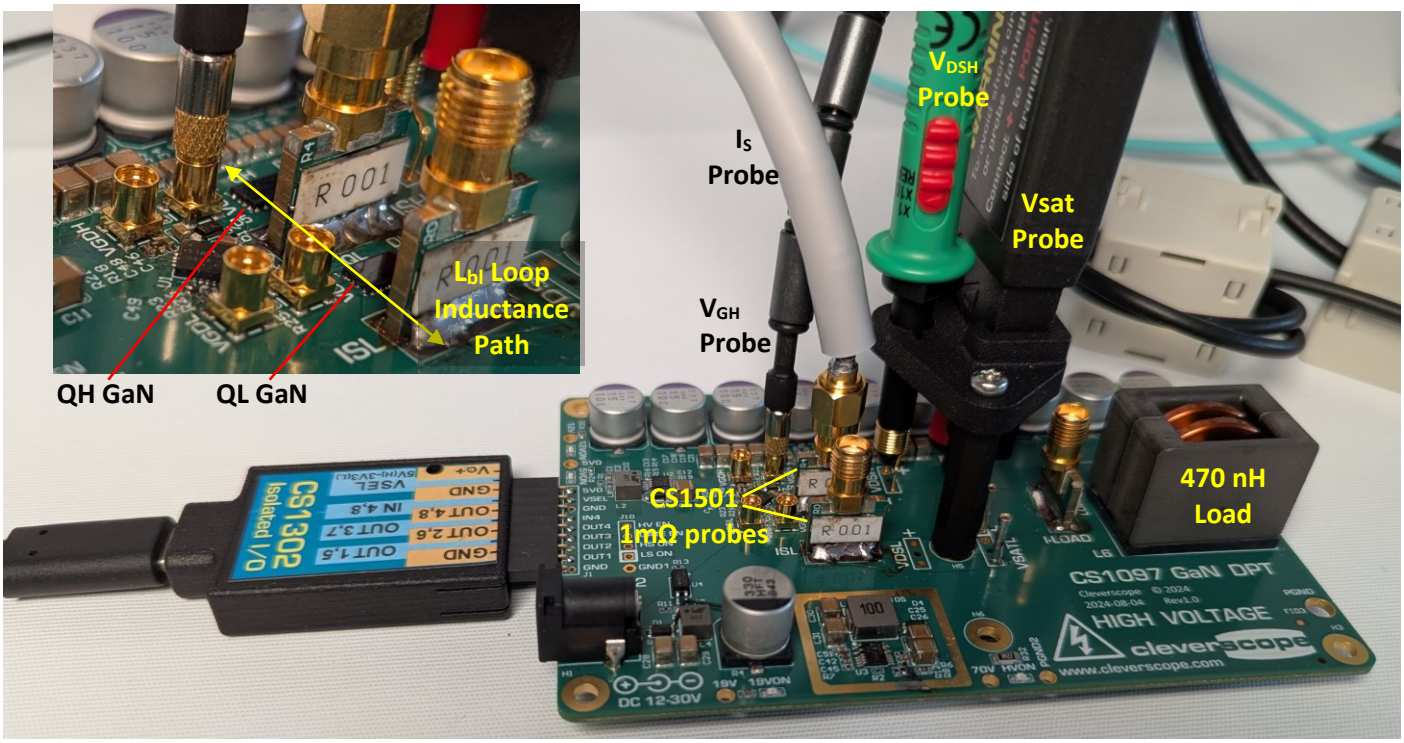
The measurements, all on the high side, are:

- Current $\mathbf{I_{SH}}$ is measured with **CS1201** Current Digitizer connected to a **CS1501** current sensor in position ISH
- Voltage $\mathbf{V_{DSH}}$ is measured with a **CS548**oscilloscope and a x10 probe fitted to the VDSH jumper.
- The Gate drive voltage $\mathbf{V_{GH}}$ is measured with a **CS1200** Voltage Digitizer connected to the G_H MMCX connector.
- The transistor saturation voltage $\mathbf{V_{SATH}}$ is measured with a **CS1133** Vsat probe plugged into the **CS548**.

The products are described in *CS548 System Specification v1.92.pdf* or later.

The total system, all measurements are the high side:





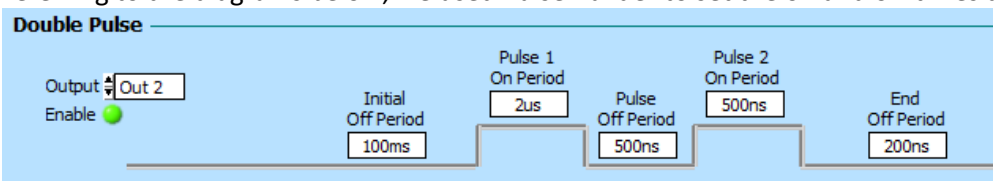
Use the **CS1302** Output Pod to drive the gate signals on the CS1097 board. OUT2 is driving the High Side gate. Use Pulse Builder to set the double pulse settings. See next section.

Double Pulse Test Discussion

The Double Pulse Test (DPT) is used to measure important parameters of either transistor of a Half Bridge switch. The measurements can be made on either the low side, or the high transistor. The low side can be measured with a standard oscilloscope. The high side requires non-ground referred measurements, and as rise and fall times become less than 50 ns, the measuring system needs very high common mode rejection. This is especially true for SiC FET and GaN FET transitors as rise and fall times may be ns. In this situation fiber isolated measuring systems must be

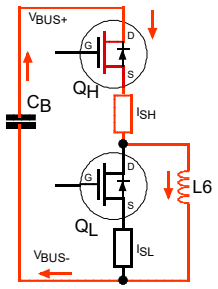
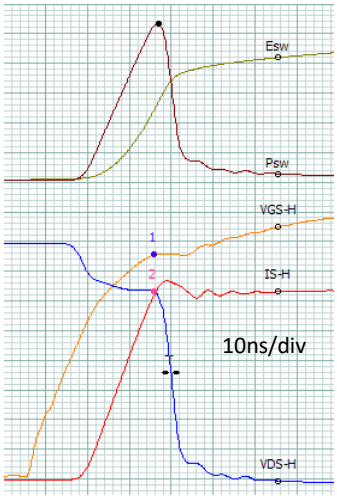
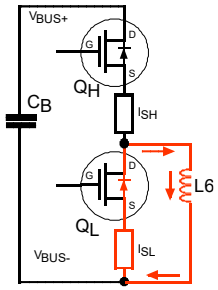
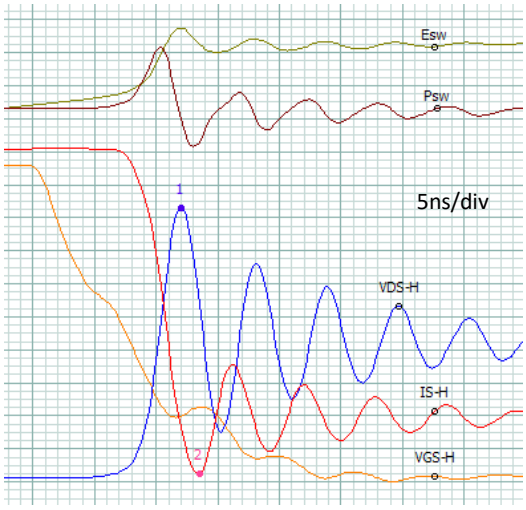
used. An inductive load and double pulse test is used to set the current at which the transistor (QH for the high side) turns off, and then turns back on. The beauty of the DPT is that after having chosen an inductor, the current is set just varying the transistor on period to reach the desired operating current.

Referring to the diagrams below, we used Pulse Builder to set the on and off times as:



Using the equation $V = L\frac{di}{dt}$, we can re-arrange to $dt = L\frac{di}{V}$. With a fixed V (about 42V in this example), and L (470 nH) we find $dt = 470n\frac{di}{42}$. Say we want to get to 180A, dt = 2.014 us. In our example we use 2us.

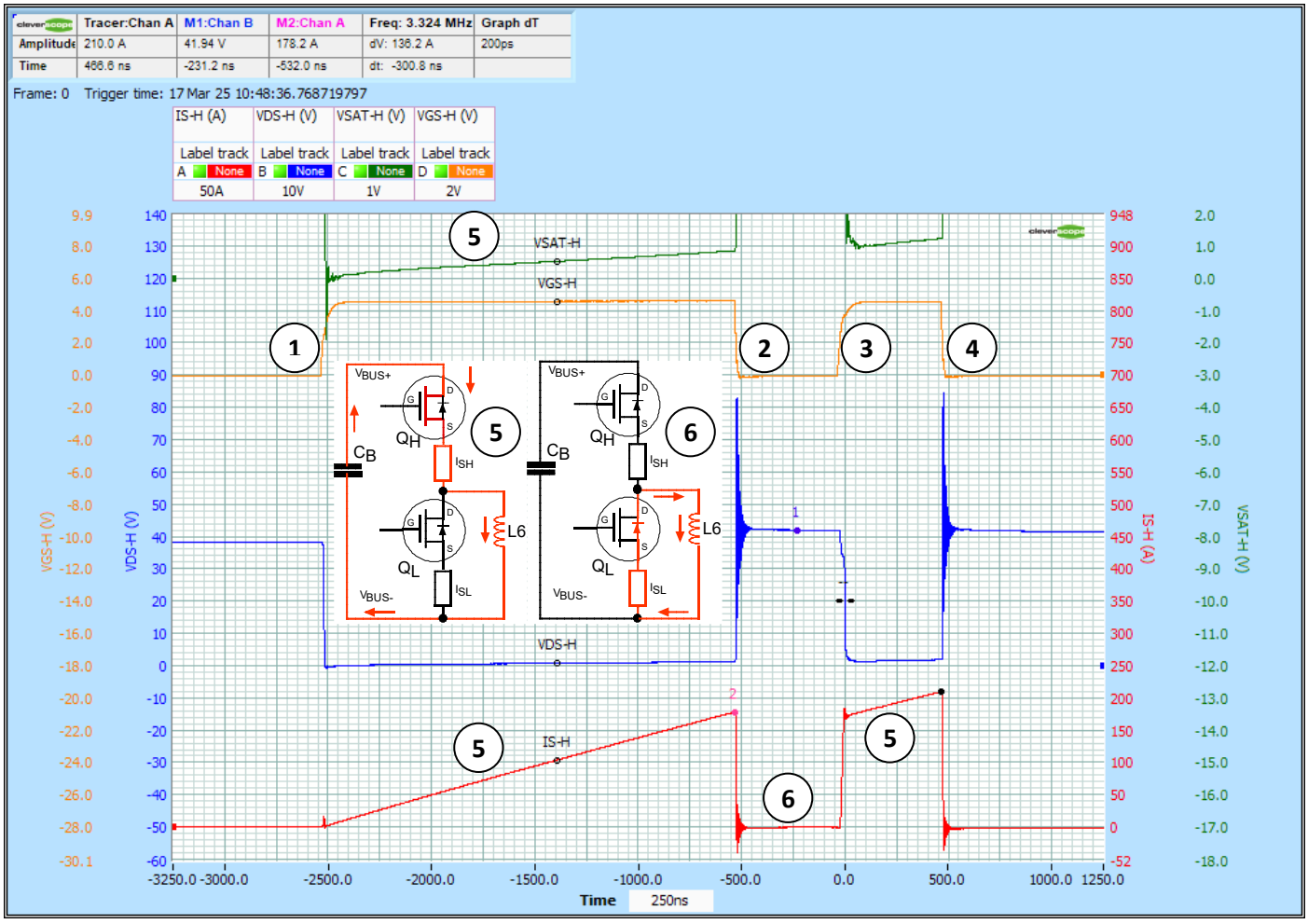
All these measurements are on the high side. There are two circumstances:

Active transitor	Current Flow	Notes
The upper transistor, QH		When transistor QH is turned on, current will flow in the *QH – L6 - CB* loop as shown.  During the transition, the $I_{S\text{-}H}$ current circulating in the *QL – L6* loop will switch to the upper transistor, rising at a rate set by the bus loop inductance, L_{bl}. Once the transistor is fully on (Marker 2), $V_{DS\text{-}H}$ will start falling, controlled by the voltage dependant Miller capacitive divider. During this time $V_{GS\text{-}H}$ plateaus, starting at Marker 1. The transition entails loss P_{SW}, which integrates as E_{SW}.
The lower transistor QL: GaN device reverse operation (3rd Quadrant), or reverse diode in parallel with QL		When transistor QH is turned off, current will flow in the *QL – L6* loop as shown.  During the transition, the voltage will rise because of L_{bl} , and resonate with the output capacitance C_{QH}. $I_{S\text{-}H}$ lags $V_{DS\text{-}H}$ by 90 degrees, and can be used for time alignment (Markers 1 – 2). The transition entails loss P_{SW}, which integrates as E_{SW}. The $V_{DS\text{-}H}$ oscillation impresses on V_{GH} based on the Miller divider, which is voltage dependant.

We can derive L_{bl} , C_{QH} , the losses, and various Gate drive values as shown in the next section.

Measurements

This is the full double pulse, over 3us:



Using the Tracer and Marker values in the information area above the graph, we see:

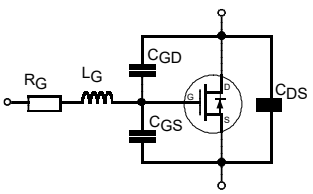
- The Bus Voltage is Marker 1, 41.94V. We used a low voltage to protect people using the board from shock.
- The Peak Current after the first pulse is Marker 2, 178.2A. The peak after the second pulse is 210.0 A (measured by the Tracer
- The Saturation voltage at the end of the first pulse is 937.7 mV

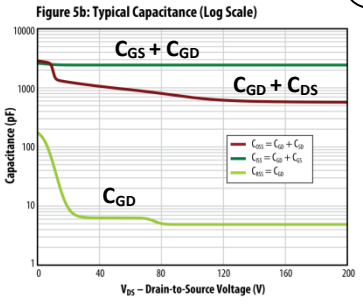
The transistor states are:

- QH was off, and is turned **on** at Edge 1.
- QH is turned **off** at Edge 2. Here, Time Align V_{DS} and I_S (2), by observing the I_S oscillation lags the V_{DS} oscillation by 90 degrees. In addition calculate $\mathbf{C_{QH}}$ once $\mathbf{L_{bl}}$ has been calculated in Edge 3.
- QH is turned **on** at Edge 3. If there is any freewheeling current from the Inductor L6 it flows reverse through QL in third quadrant mode. I_{SL} senses the freewheeling current. On the edge calculate $\mathbf{L_{bl}}$
- QH is turned **off** at Edge 4.
- In State (5) QH is on. Current flows from the Bus Capacitor CB through QH, and through L6 and returns to CB. I_{SH} senses the load current.
- In State (6) QH is off. Current is free wheeling through reversed QL and L6.

In this discussion $\mathbf{L_{bl}}$ represents the combined inductance of every series connected track/device in the power loop (5)

The transistor model can be simplified as on the right. Note that $\mathbf{C_{GS}} + \mathbf{C_{GD}}$ is constant, but the ratio of the $\mathbf{C_{GD}} - \mathbf{C_{GS}}$ divider varies as $\mathbf{C_{GD}}$ varies with V_{DS}. This divider is responsible for the flat Miller Plateau. When QH is off, the output capacitance is $\mathbf{C_{GD}} + \mathbf{C_{DS}}$. See the graph for the capacitor relationships with V_{DS}.

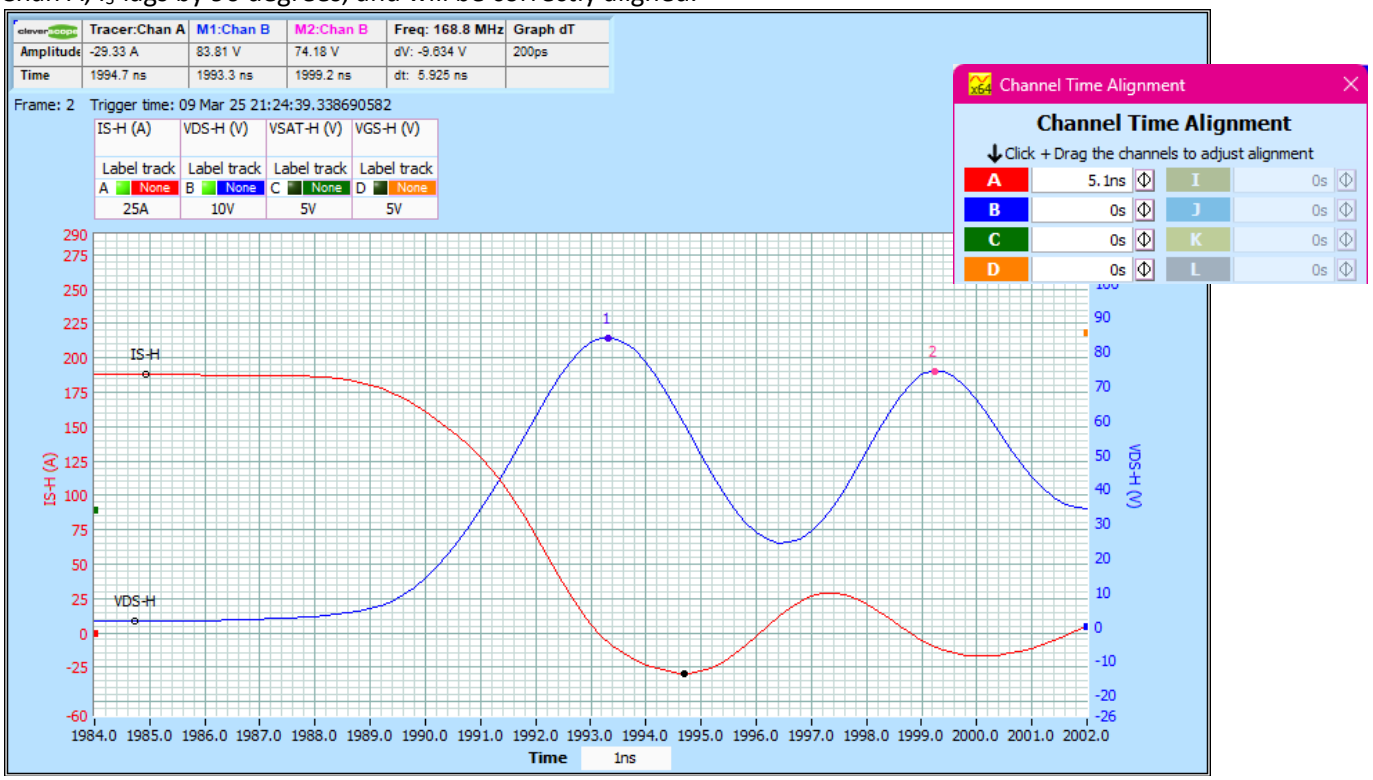




The Circled numbers refer to Edges and States of measurements we make in the following sections.

(2) Ensure Current and Voltage waveforms are correctly aligned.

An inductive current lags a resistive voltage by 90 degrees. When the bus loop inductance **L_{bl}** resonates with the QH output capacitance, **I_S** will lag **V_{DS}** by 90 degrees. With the Channel Time Alignment function set to 5.1ns on Chan A, I_S lags by 90 degrees, and will be correctly aligned.

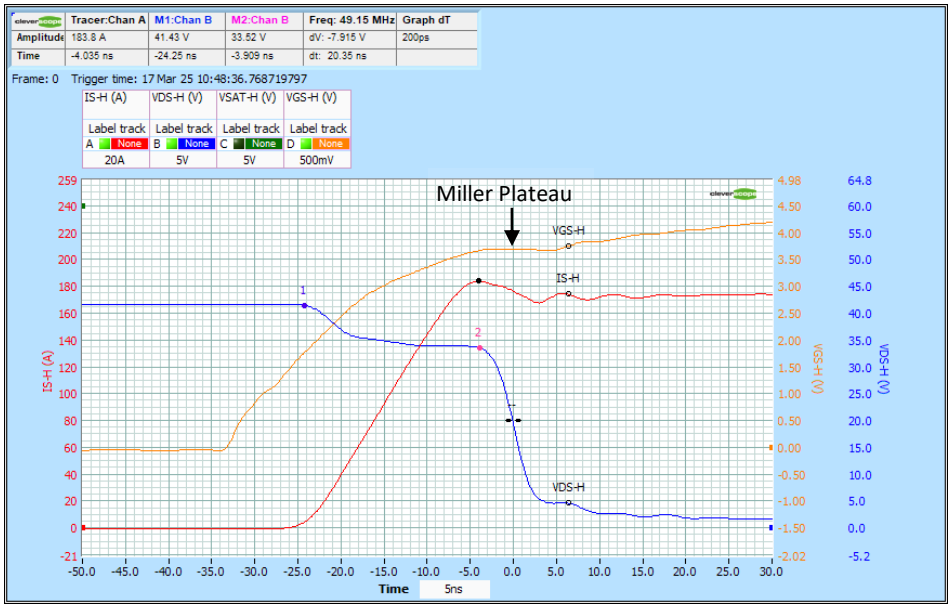


Period Marker 1 -2 = 5.925ns. 90 deg is ¼ of this, or 1.481ns. The tracer shows the current negative peak at 1994.7ns, which is 1994.7 – 1993.3 = 1.4ns. This is 81ps too early, but good enough!

(3) Measure the bus loop inductance

When the upper transistor QH turns on the load current ramps up causing a voltage drop across the bus loop inductance **L_{bl}**. This is seen as a dip on **V_{DSH}**. The equation $Vds = Vdc - \mathrm{Lbl}\frac{di}{dt}$ can be rearranged as $\mathrm{Lbl} = (\mathrm{Vdc} - \mathrm{Vds})\frac{dt}{di}$ Plugging in Marker 1 – Marker 2 = 7.91V, dt = 20.35ns, and di = 183.8A (tracer, and markers area)

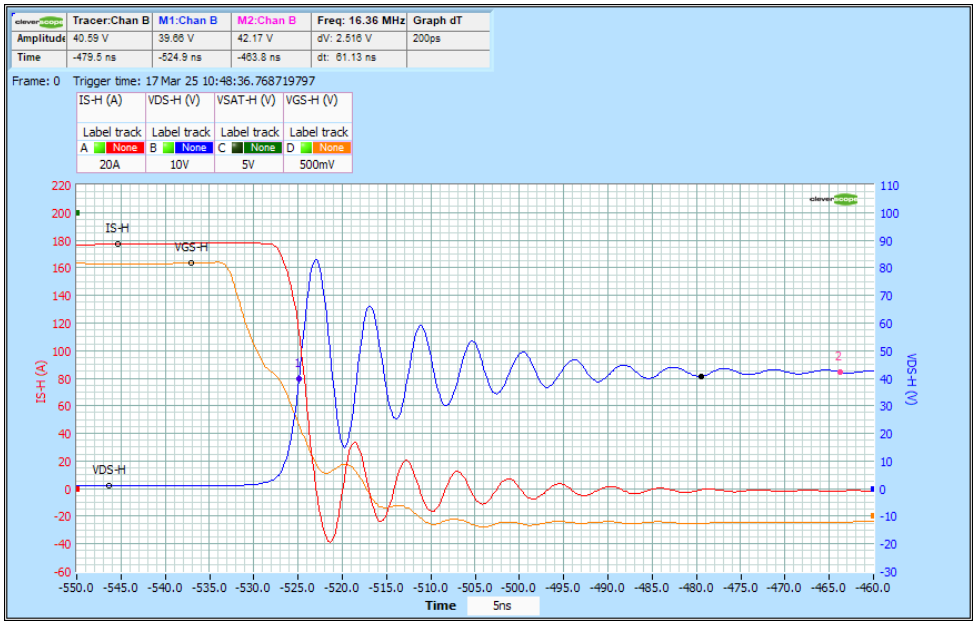
L_{bl} $= (7.91)\frac{20.35n}{183.8}$ = 876 pH (Note that there is a contribution from the two current sensors in this).



Once the current rise has finished and the transistor is fully on, **V_{GSH}** stops increasing, and **V_{DSH}** starts to drop rapidly. The voltage across the capacitance **C_{GD}**, which corresponds to the feedback capacitance Crss in the data sheet drops as well. The capacitance **C_{GD}** is voltage dependant – increasing with reducing voltage. This keeps **V_{GS}** constant, and is called the Miller Plateau. The feedback capacitance is also called the Miller capacitance.

2 Measure the transistor output capacitance

When QH is turned off, the bus loop inductance $\mathbf{L_{BL}}$, and the transistor output capacitances $\mathbf{C_{QH}} = \mathbf{C_{GD}} + \mathbf{C_{DS}}$ for both transistors form an LC tank which resonates. The resonant frequency is $f = \frac{1}{2\pi\sqrt{LC}}$ so $\mathbf{C_{QH}} = \frac{1}{(2\pi f)^2\,\mathbf{Lbl}}$. We use the Markers to delineate the oscillation:

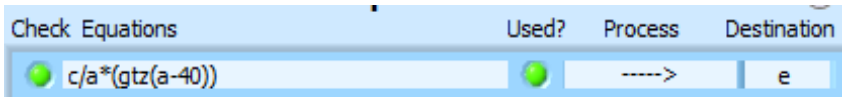


Tracker Info	Chan A	Chan B
Label	IS-H	VDS-H
Fundamental Frequency	174.0 MHz	174.4 MHz

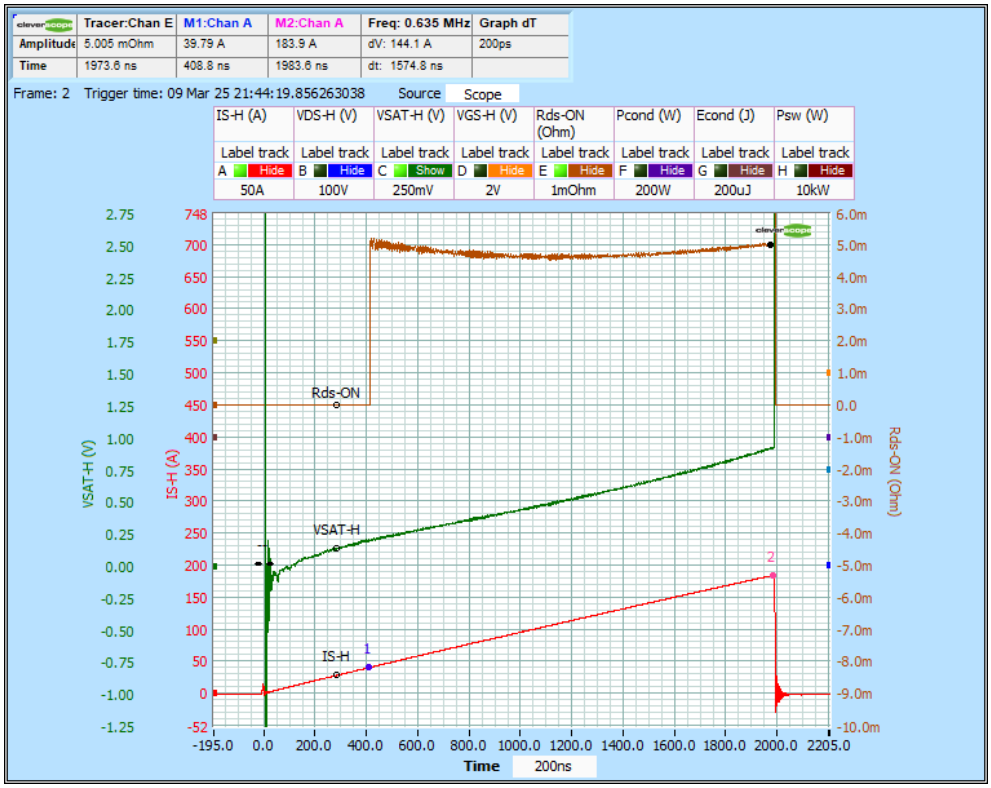
The oscillation frequency is 174.4 Mhz. Thus C = $\frac{1}{(2\pi\ 174.4M)^2\ 876p}$ = 950pF. The EP2304 data sheet shows an output capacitance of 704 – 1010 pF, dependant on voltage.

3 Calculation of R_{DSON}.

R_{DSON} is Vsat/Is. We use the Maths Equation Builder to calculate this. To avoid incorrectly high values of R_{DSON} we only calculate it when $\mathbf{I_S}$ is greater than 40A. This is the Maths equation:



Channel C is Vsat, and Channel A is Is.



We calculate about 5mOhm, which agrees with the data sheet.

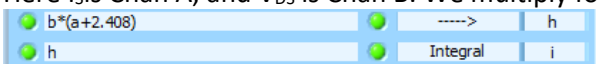
Chan E is used to display R_{DSON}.

Chan C is V_{SAT-H}.
Chan A is I_{SH}

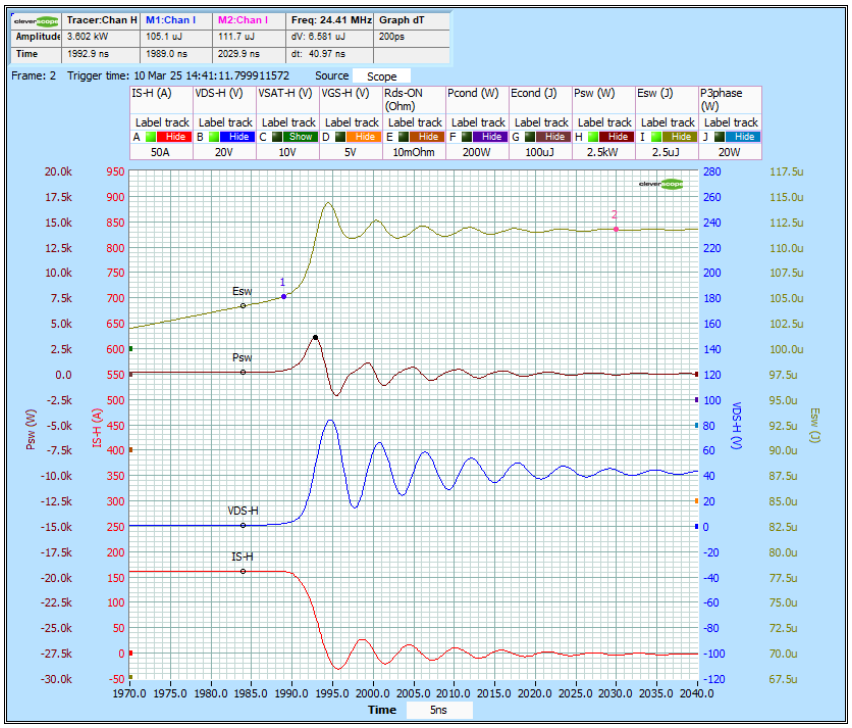
2 Turn Off Measurement of Switching power and energy

The Switching Power and Energy are measured using the Maths Equation Builder.

Here $I_S$is Chan A, and V_{DS} is Chan B. We multiply for power and then integrate for energy.



Time alignment is crucial as **I_S** lags **V_{DS}**. We measure:



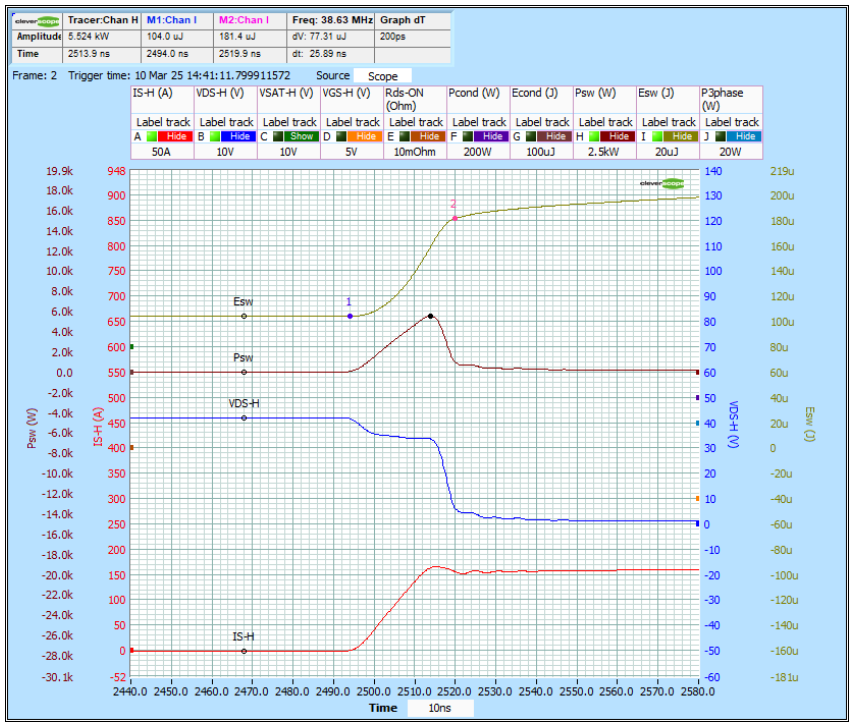
The 10-90% edge times are measured by signal information as:

Tracker Info	Chan A	Chan B
Label	IS-H	VDS-H
Pulse 0->1 Time	3.242 ns	2.042 ns

The energy is oscillatory during the resonance. We wait until it settles down (in about 40ns). The peak power is 3.6kW (Tracer), and Marker 2 – Marker 1 give a total energy change of 6.581uJ. Were this falling switch event to happen at 100 kHz, the falling edge switch energy would be 100kHz x 6.581uJ = 0.658W.

3 Turn On Measurement of Switching power and energy

We use the same equation to measure Power and Energy:



The 10-90% edge times are measured by signal information as:

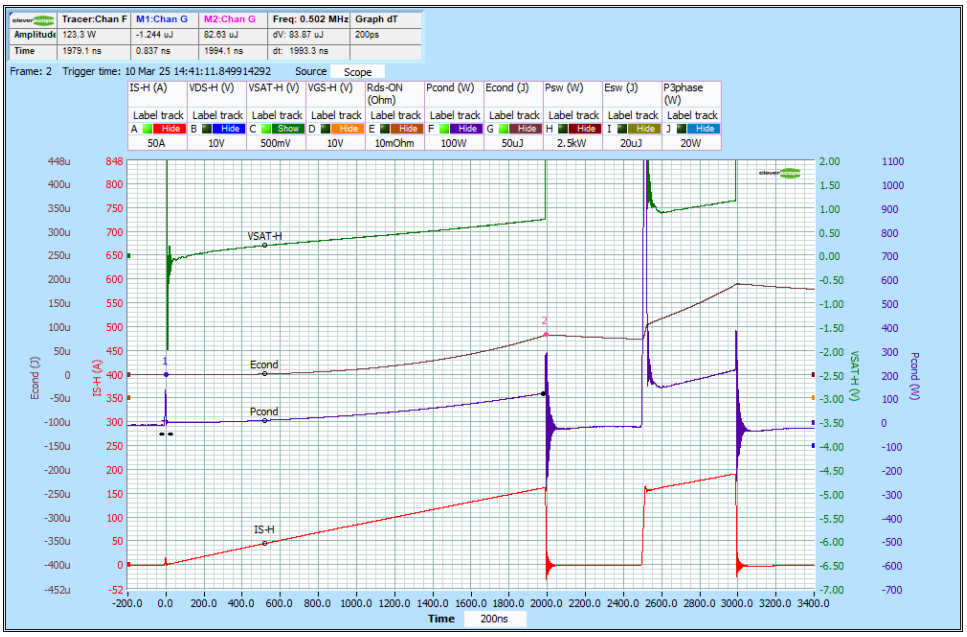
Tracker Info	Chan A	Chan B
Label	IS-H	VDS-H
Pulse 0->1 Time	13.36 ns	22.48 ns

At turn on the Switch energy is 77.31uJ. After this the energy keep rising because QH is conducting. The peak switch power is 5,524 kW. Operating at 100 kHz, the rising edge power would be 0.7731W.

5 Conduction Energy

The conduction energy is the total energy over one conduction cycle. In our example, the conduction cycle is only 2us. We calculate P = V_{SAT-H} I_S Channel A is I_S, Channel C is V_{SAT-H}. The Maths equation is:

Line 1 calculates the Power, and line 2 Integrates it to find Energy. The results are:



The Tracer gives the peak power as 123.3W.

The Energy is 83.87uJ (Marker 2 – Marker 1).

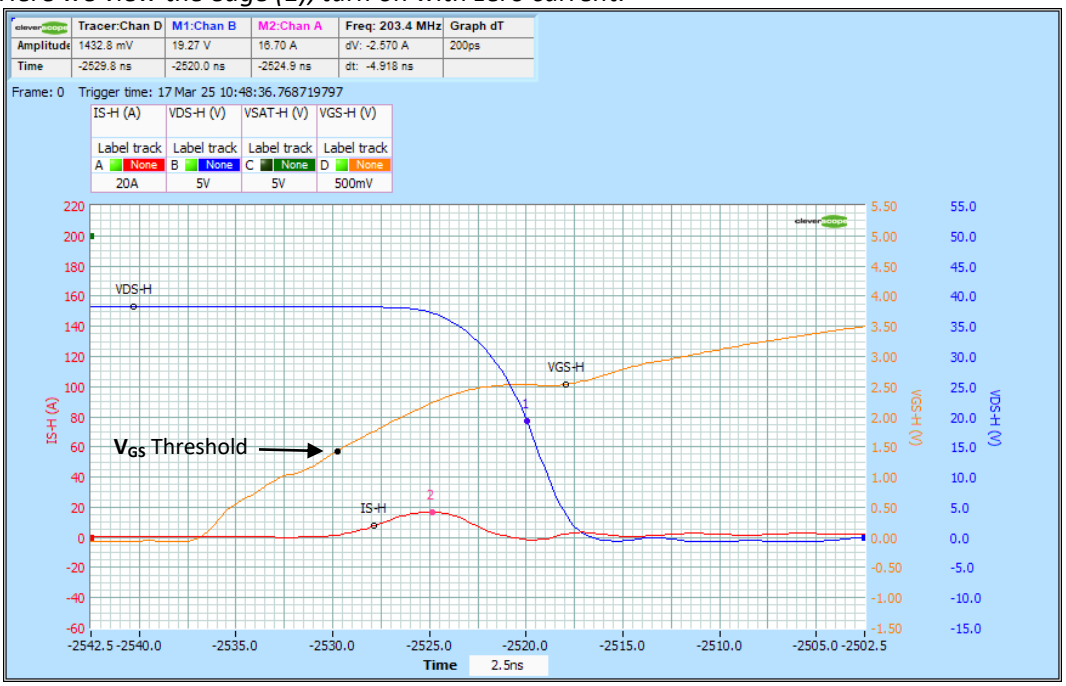
If this 2us pulse repeated at a 100kHz rate, the total power would be 0.8387W.

Total Power would be about 0.84+0.66+0.77 = 2.27W. QH would be getting pretty hot!

- **Gate Drive**

  We compare the VGS with VDS and IS to determine alignment between all the signals, the Vgs threshold, the Miller Plateau, and performance of our gate drive chip.

1 *Here we view the edge (1), turn on with zero current.*



a. The $\mathbf{V_{GS}}$ threshold, at which current first starts rising is the tracer, at 1.43V, close to 1.5V typical.

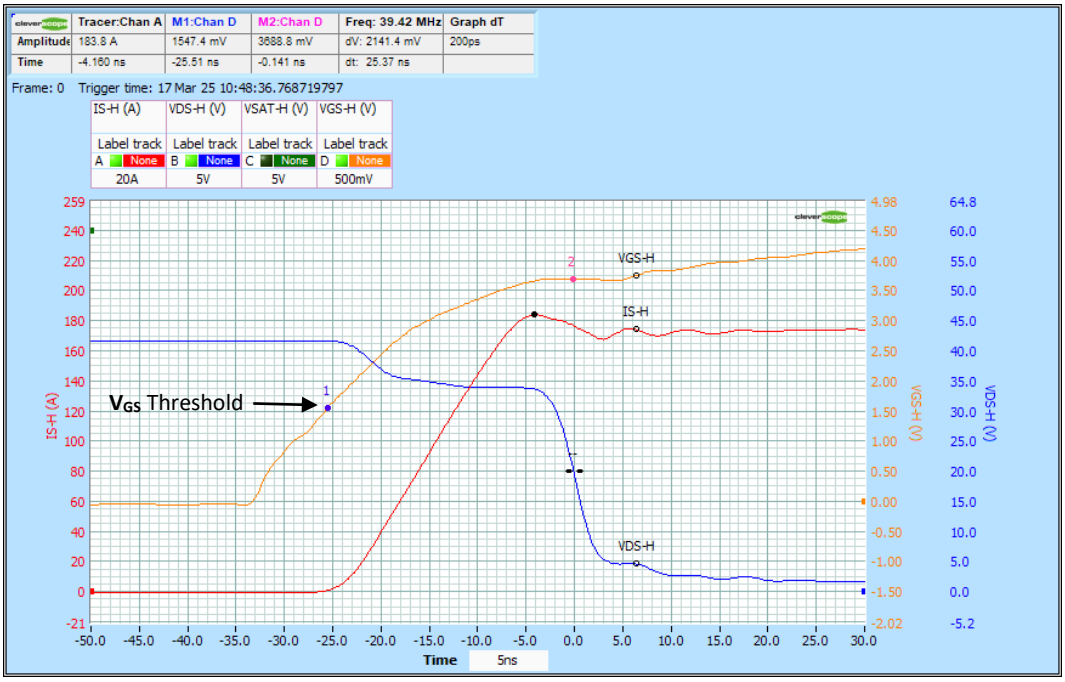
b. The current peak, 16.7A, is the peak current that flows through $\mathbf{L_{BL}}$, as QH is turned on.

c. The Miller Plateau is clearly visible as $\mathbf{V_{DS}}$ falls, at about 2.5V.

d. Rise and fall times are:

Tracker Info	Chan A	Chan B	Chan D
Label	IS-H	VDS-H	VGS-H
Pulse 0->1 Time	2.196 ns	5.180 ns	50.94 ns

(3) *Here we view the edge (3), turn on with high current:*



a. The VGS threshold looks to be about 1.55V (Marker 1), , close to 1.5V typical in the data sheet.
b. The Miller Plateau has raised to 3.69V at the much higher on current.
c. Rise and falls times are extended due to **L_{BL}** charge time:

Tracker Info	Chan A	Chan B	Chan D
Label	IS-H	VDS-H	VGS-H
Pulse 0->1 Time	13.51 ns	23.42 ns	51.85 ns

d. Our gate drive chips is taking it's time! However the turn on time is limited by **L_{BL}**.

Summary of Measurements Made

We made these measurements:

Measurement	Value	Comment
Chan A, I_S time alignment	5.1ns	Set using Channel Time Alignment menu item
Bus Loop Inductance	Total 876pH	This will be reduced if the two CS1501 current sensors are not fitted (they contribute 163 pH each, but the pads for them remain).
QH output capacitance	950 pF	In the data sheet range of 704 – 1010pF.
R_{DSON}, QH on resistance	4.8 – 5mΩ	Data sheet typical value is 3.5mΩ to 5mΩ max. Our design was not entirely 4 wire, and we think this has elevated the value a bit.
Turn Off switch Energy	6.58uJ	With 183.8A turn off
Turn On switch Energy	77.31uJ	With 183.8A turn off
Turn Off VDS rise time	2.04 ns	10-90% measurement
Turn Off IS fall time	3.24 ns	10-90% measurement
Turn On VDS fall time	23.42ns	10-90% measurement, includes Bus Loop Inductance charge time.
Turn On IS rise time	13.51ns	To 183.8 A
Conduction energy	83.87uJ	From 0 to 183.8A in 2us.
VGS Threshold voltage	1.55V	At 180 A turn on. Data sheet typical is 1.5V.
VGS plateau	2.5V to 3.69V	Operating at 0 or 180A **I_S**

A panel to make it easier to automatically make all these measurements is in development.

Conclusion

The CS548 system, including CS1201 current sensor, and CS1133 Vsat probe can be used to do a Double Pulse Test (DPT) on a GaN or other transistor, on both the high side, and low side. Results are in agreement with the device data sheet.